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Claims

[c1] A device comprising:
a substrate comprising a silicon-containing layer atop an insulating layer;
at least one trench within said substrate, said at least one trench comprising a divot laterally extending from a trench sidewall into said insulating layer;
a capacitor in a lower portion of said at least one trench, and
a transistor in an upper portion of said at least one trench, said transistor in electrical contact to said silicon-containing layer of said substrate through an upper strap diffusion region partially positioned within said divot.

[c2] The device of Claim 1 wherein said divot comprises doped polysilicon.

[c3] The device of Claim 1 wherein said transistor and said capacitor are separated by a trench top oxide layer.

[c4] The device of Claim 3 wherein said transistor comprises a gate region, said gate region comprising a gate dielectric formed on sidewalls of said upper portion of said

trench and a polysilicon gate formed atop said trench top oxide layer.

[c5] The device of Claim 4 wherein said transistor further comprises a source and a drain, said drain being a lower strap diffusion region positioned to provide electrical communication between said transistor and said capacitor, said source being said upper strap diffusion region.

[c6] The device of Claim 5 wherein said drain and said source comprise a first conductivity-type dopant and a portion of said substrate positioned between said drain and said source is doped with a second conductivity-type dopant.

[c7] The device of Claim 4 wherein said substrate further comprises an array region and a support region separated by an isolation region, said array region including said at least one trench and said support region comprising logic devices, said logic devices comprising polysilicon gate devices having logic source/drain regions formed in said silicon containing layer.

[c8] The device of Claim 6 wherein said array region further comprises active wordlines in electrical communication with said transistor in the at least one trench, wherein electrical communication is provided through a transistor junction within said at least one trench and contacting

said gate region of said transistor.

[c9] The device of Claim 1 wherein a bitline contacts said silicon-containing layer and is in electrical contact to said transistor through said upper strap diffusion partially positioned in said divot in said buried insulator layer.

[c10] The method of Claim 1 wherein said divot is on one side of the trench.

[c11] A method for forming a transistor comprising:
forming at least one trench in a silicon-on-insulator substrate, said at least one trench formed to a depth extending through an insulating layer of said silicon-on-insulator substrate;
forming a node dielectric and collar in said at least one trench, said collar being positioned above said node dielectric;
forming a capacitor node in a lower portion of said at least one trench;
recessing said collar below a top surface of said capacitor node to expose a portion of said insulating layer and laterally etching said insulating layer to provide a divot;
forming strap diffusion regions, said strap diffusion regions comprising a lower strap diffusion region partially positioned on said collar and an upper strap diffusion region partially positioned in said divot;

depositing a trench top oxide on said capacitor node; and

forming a gate region atop said trench top oxide.

[c12] The method of Claim 11 wherein forming at least one trench comprises:

forming a patterned pad dielectric layer exposing portions of said silicon-on-insulator substrate; and

etching exposed portions of said silicon-on-insulator substrate selective to said patterned pad dielectric layer.

[c13] The method of Claim 12 wherein recessing said collar comprises a directional etch process that recesses said collar selective to said patterned pad dielectric layer and said capacitor node.

[c14] The method of Claim 12 wherein laterally etching said insulating layer comprises a non-directional etch that removes a portion of said insulating layer abutting said at least one trench to provide said divot selective to said patterned pad dielectric layer and said capacitor node.

[c15] The method of Claim 14 where said non-directional etch comprises a chemical dry etch process including CF_4 feed gas, a wet chemical etch including NH_4OH or combinations thereof.

[c16] The method of Claim 12 wherein forming strap regions

comprises

depositing polysilicon within said at least one trench;

etching polysilicon selective to said patterned pad dielectric layer, wherein a portion of said polysilicon remains atop said collar being coplanar with a top surface of said capacitor node and wherein a portion of said polysilicon remains within said divot.

[c17] The method of Claim 11 wherein said gate region comprises a thermally grown gate dielectric on an upper portion of said at least one trench and a polysilicon gate region.

[c18] The method of Claim 11 further comprising forming an interconnect atop said gate region, said interconnect comprising insulating sidewall spacers and a conductive plug.

[c19] The method of Claim 18 further comprising:

forming a patterned wiring dielectric layer atop said silicon-on-insulator substrate, wherein said patterned wiring dielectric layer exposes another portion of said silicon-on-insulator substrate;

etching said another portion of said silicon-on-insulator substrate to form an isolation region, wherein said isolation region separates an array portion of said silicon-on-insulator substrate from a support portion of said

silicon-on-insulator substrate, said array portion comprising said at least one trench;
stripping said patterned pad dielectric layer and said patterned wiring dielectric layer to expose said support region of said silicon-on-insulator substrate; and
forming logic devices in said support region.

[c20] The method of Claim 19 further comprising forming wordlines in said patterned wiring dielectric layer, wherein said wordlines contact said interconnect, and forming a bitline to an upper silicon-containing layer of said silicon-on-insulator substrate, wherein said bitline is in electrical contact with said upper strap through said buried insulator layer.